DESIGN AND FABRICATION OF GaAs ANALOG-TO-DIGITAL ICs

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ABSTRACT

Some RADAR systems require 2- or 3-bit ADCs operating at several hundred megahertz to gigahertz sampling rates. Earlier, we have shown that GaAs MESFET comparators can meet both the speed and resolution requirements of such A/Ds. A 3-bit A/D circuit was designed and optimized. ICs were fabricated and successfully operated from dc through giga-sample per second rate.

A. INTRODUCTION

Griffiths[1] has shown that major improvements can be made in RADAR system performance if 2- or 3-bit A/Ds operating at several hundred MHz are available. Degraaf et al.[2] have reported silicon bipolar-based A/Ds operating in the 300-400 MHz range. Their power dissipation is high and there is no possibility of increasing the sampling rate. Upadhyayula[3,4] has described GAAs MESFET comparators suitable for gigabit-rate analog-to-digital converter applications. Based on this principle, 2- and 3-bit A/D circuits were designed, fabricated, and evaluated. The performance of 2-bit A/Ds has been studied at sampling rates at high as 1.0 GHz. The smallest pulse width sample/hold type input digitized is 500 ps. Three-bit A/Ds are currently being evaluated.

B. CIRCUIT DESIGN

Two- and three-bit A/Ds consisting of comparators and decoding logic circuits were designed. The quantization step Q for the A/D is given by

$$Q = \frac{\text{Full scale input voltage}}{(2^n - 1)}$$

where n is the number of bits. The theory of GaAs MESFET comparators was reported earlier by Upadhyayula[3]. An overdrive voltage of 80-100 mV is required for MESFET comparators[3]. Therefore, quantization steps of 0.4 V and 0.2 V were selected for 2-bit and 3-bit A/Ds, respectively. A full-scale input voltage available is about 1.0-1.5 V. Figure 1 shows the circuit of a 3-bit A/D. A gray code output was chosen because of its smaller processing delay and lower circuit complexity. Eight parallel voltage comparators are used at the input and these can be seen at the bottom of the schematic shown in Fig. 1. The 3-bit outputs and the overrange bit are seen at the top of the circuit following the decoding logic. The thresholds for the eight comparators are 0.2 V apart and were achieved by an appropriate choice of the ratios of the widths of load to the switching FETs in the comparators. After preliminary design, the circuit was computer simulated to determine the optimal configuration for the decoding logic and to determine the potential performance.

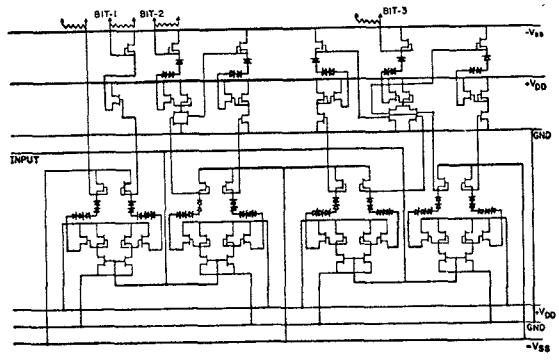

Fig. 1. Schematic of a 3-bit A/D. Comparators are shown in the bottom section and decoding logic in the top section.

The circuit model[5] for the MESFET is contained in a subroutine developed for use with R-CAP, a powerful circuit simulation program. This model accurately describes the GaAs drain MESFET current-voltage characteristics, includes transit-time delay effects, and provides voltage dependent gate-source capacitance. MESFET parameters not directly measurable are acquired from two-dimensional MESFET simulation.[5]

The longest settling time in the 3-bit A/D is associated with bit-3, the lowest order bit. In the worst case, as many as four comparators may change states before an output os produced. Circuit simulation showed that a decoding logic sequence of INVERTOR-OR-NAND gates resulted in shorter settling time than an INVERTOR-AND-NOR logic sequence. Figure 2 shows the INVERTOR-OR-NAND logic configuration for the bit-3 circuit. The inverters follow the fastest switching comparators and help balance the parallel signal delays. The comparator outputs are combined to provide Gray-code outputs. Assuming that 1, 3, 5 and 7 are the outputs of the first,

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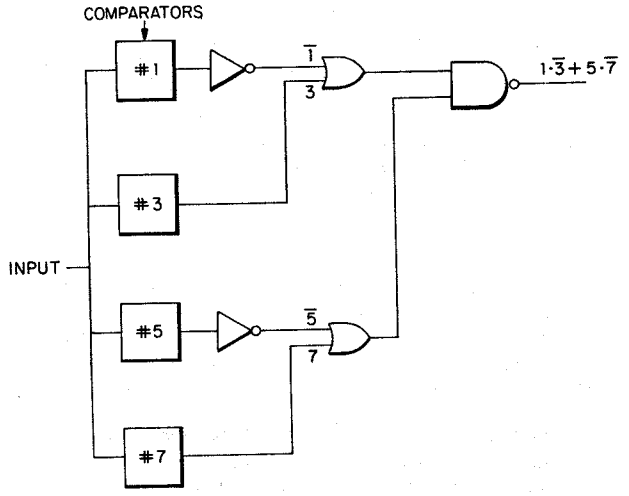


Fig. 2. A/D converter logic for bit-3 output voltage.

third, fifth and seventh level comparators, the bit-3 (2°) output is $1.\overline{3} + 5.\overline{7}$, which by DeMorgan's theorem is the same as $(\overline{1+3})\cdot(\overline{5+7})$.

The simulation is made assuming all MESFETs in the comparators have a 5 V pinchoff voltage and all MESFETs in the decoding section have 3 V pinchoff voltages. Characteristics of our 1-μm gate length GaAs MESFETs have been assumed. The input signal to the comparators (from a sample-and-hold) circuit) is a voltage step with 80 ps rise time.

Figure 3 shows the input and output waveforms for the bit-3 circuit simulation for two cases. The proper output is a logic high for -0.4 V input and a logic low for -0.6 V input. The bit-3 output can be seen to settle after about 500 ps. The longest settling time for any input voltage level is about 550 ps. This circuit is therefore capable of processing samples at the rate of 1 GHz or higher.

C. IC FABRICATION

The procedure used in the fabrication of GaAs ICs closely follow that for GaAs power MESFETs. Recessed gate MESFETs with 1.0 um gate-length were used. Au:Ge/Ni/Au ohmic contacts and Ti/Pd/Au Schottky barriers were used. To obtain uniform device currents and pinchoff voltages, the wafers were electrolytically-thinned to the limit before IC fabrication. Two-level metal interconnections are required to complete the integrated circuit fabrication. PI-2555A polyimide served as dielectric isolation layer. PI-2555A has a low (250°C) curing temperature and is compatible with GaAs device processing. Two- and three-bit GaAs analog-to-digital converter ICs were fabricated. Figure 4 shows a photomicrograph of a completed 3-bit IC. The chip size is 1.3 mm x 1.05 mm.

D. RESULTS

Sample/hold and D/A circuits operating at gigabit-rates are not available. The following test procedure was therefore employed for IC evaluation. DC biases for the comparator and coding logic

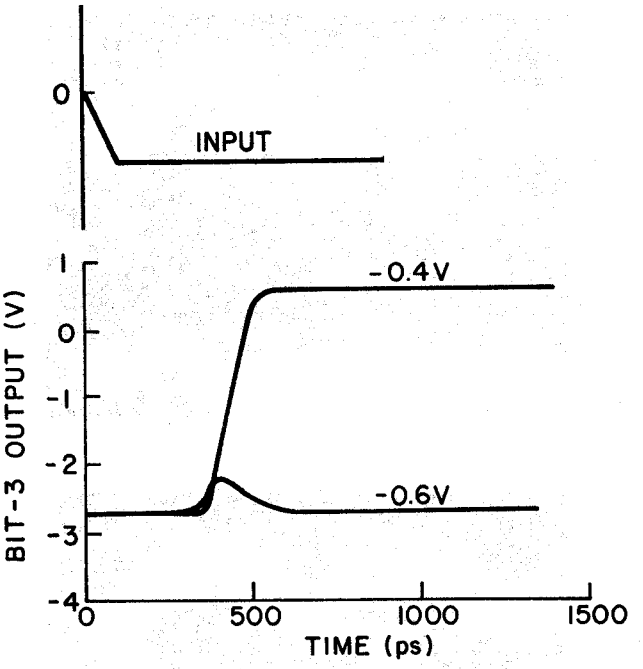


Fig. 3. Input waveform and BIT-3 output voltage as a function of time from R-CAP simulation for input pulse amplitudes of -0.4 V and -0.6 V.

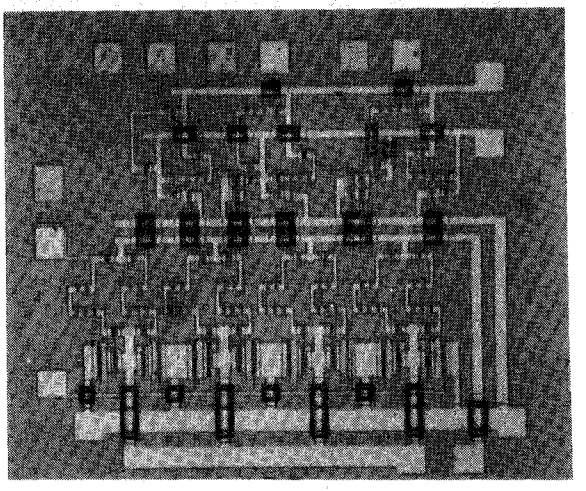
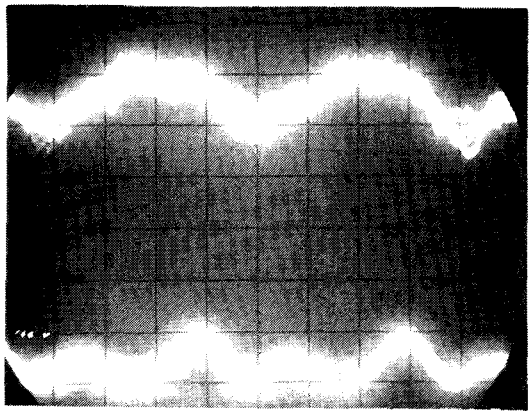


Fig. 4. Photomicrograph of a 3-bit A/D IC chip.

circuits were optimized. A variable input voltage pulse ranging from 0 to -1.5 V was applied to the comparators. Input pulse width and repetition rates were independently varied. The pulsewieth simulates a sample/hold input and the repetition rate corresponds to the sampling rate. The outputs were monitored on a sampling scope. The 2-bit A/D chip was operated from dc to 1.0 GHz sampling rate. Some preliminary results were reported[6] recently. The 3-bit A/D ICs have also been successfully evaluated up to giga-sample per second rate. The response of the 3-bit A/D LSB to a 600-700 ps wide input pulse is shown in Fig. 5. When the input is

(a)



(b)

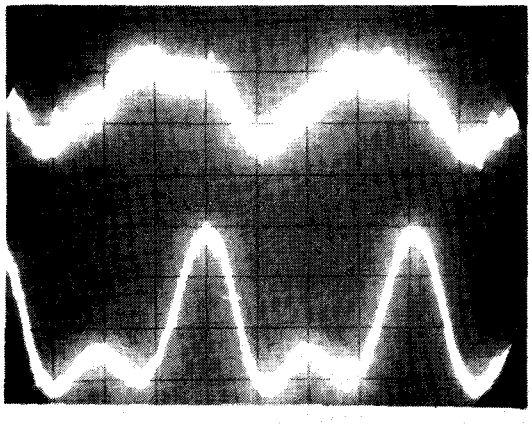


Fig. 5. Bit-3 response for a 600-700 ps input pulse. Top trace: input 44 mV/div. Bottom trace: output 500 mV/div. Horizontal scale: 500 ps/div.

below threshold for comparator 1, the output is zero (Fig. 5a). When the input is increased above the threshold level, logic "1" is produced (Fig. 5b). This clearly demonstrates that the response time of the comparators and coding logic is less than 600 ps. This result is in good agreement with the computer simulations discussed above.

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